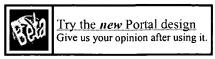
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_	66	703/19.ccor.	USPAT;	2003/07/11 18:03
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-	25	netlist adj model	USPAT;	2003/06/25 12:30
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-	2	5684724.URPN.	USPAT	2003/06/25 13:08
-	7	("4901260" "5157620" "5272651"	USPÄT	2003/06/25 13:11
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_	38		USPAT	2003/06/25 16:56
_	2	virtual adj (flip-flop latch)	USPAT;	2003/07/11 18:05
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-	744	test adj pattern adj generator	USPAT;	2003/07/14 03:27
			US-PGPUB	
-	158	virtual adj clock	USPAT;	2003/07/14 03:28
			US-PGPUB	
-	122	(virtual adj clock) and delay	USPAT;	2003/07/14 03:28
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-	95	((virtual adj clock) and delay) and	USPAT;	2003/07/14 03:28
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-	1	("6009531").PN.	USPAT;	2003/07/14 04:08
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ACM Transactions on Design Automation of Electronic Systems (TODAES) April 1999 Volume 4 Issue 2

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Cycle and phase accurate DSP modeling and integration for HW/SW co-verification Lisa Guerra , Joachim Fitzner , Dipankar Talukdar , Chris Schläger , Bassam Tabbara , Vojin Zivojnovic Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

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8 Browsing in chip design database

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David Gedye , Randy Katz

Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

A design browser is a tool for exploring the interconnected web of design objects managed by a CAD database. The browser described in this paper is the first such tool to present this information graphically—directed graphs are drawn to show the relationships that exist between objects in the database. Since graphs can become very large, techniques referred to as rectangular and hourglass pruning have been developed to reduce the info ...

9 Partitioned ROBDDs—a compact, canonical and efficiently manipulable representation for Boolean functions Amit Narayan , Jawahar Jain , M. Fujita , A. Sangiovanni-Vincentelli

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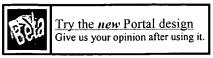
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997

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J. Koehl , U. Baur , T. Ludwig , B. Kick , T. Pflueger

Proceedings of the conference on Design, automation and test in Europe February 1998

We describe the methodology used for the design of the CMOS processor chipset used in the IBM S/390 Parallel Enterprise Server -Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm2 is comparable to the most advanced custom designs and that the impact of interconnect d ...

A BIST scheme for RTL controller-data paths based on symbolic testability analysis Indradeep Ghosh , Niraj K. Jha , Sudipta Bhawmik

80%

Proceedings of the 35th annual conference on Design automation conference May 1998

This paper introduces a novel scheme for testing register-transfer level controller/data paths using built-in self-test (BIST). The scheme uses the controller netlist and the data path of a circuit to extract a test control/data flow (TCDF) which consists of operations mapped to modules in the circuit and variables mapped to registers. This TCDF is used to derive a set of symbolic justification and propagation paths (known as test environment) to test some of the operations and vari ...

Efficient testing of clock regenerator circuits in scan designs

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Rajesh Raina, Robert Bailey, Charles Njinda, Robert Molyneaux, Charlie Beh

Proceedings of the 34th annual conference on Design automation conference June 1997

ATM traffic shaper: ATS J. C. Diaz , P. Plaza , J. Crespo 77%

Proceedings of the conference on Design, automation and test in Europe February 1998

The design and Implementation of an ATM Traffic Shaper (ATS) is here described. This IC was realized on a 0.35m CMOS technology. The main function of the ATS is the collection of low bit rate traffics to fill a higher bit rate pipe in order to reduce the cost of ATM based services, nowadays mainly influenced by transmission cost. The circuit fits in several ATM system configurations but mainly will be used at the User-Network Interfaces or Network-Network interfaces. The IC was designed with a T ...

Parallel pattern fault simulation of path delay faults

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M. Schulz , F. Fink , K. Fuchs

Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989

This paper presents an accelerated fault simulation approach for path delay faults. The distinct features of the proposed fault simulation method consist in the application of parallel processing of patterns at all stages of the calculation procedure, its versatility to account for both robust and non-robust detection of path delay faults, and its capability of efficiently maintaining large numbers of path faults to be simulated.

An intelligent module generator environment P. Six , L. Claesen , J. Rabaey , H. De Man

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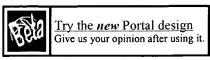
4	Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986 An environment for the generation of modules is described. It includes tools for interactive design of parameterised procedures describing the structure as well as the topology. For the layout symbolic cells are used which are automatically fitted together as defined by the topology. For the verification and characterization rule based expert tools were developed to recognize registers, check the clocking rules, find the critical path and the appropriate test patterns to calculat	
7 4	Proving circuit correctness using formal comparison between expected and extracted behaviour Jean-Christophe Madre, Jean-Paul Billon Proceedings of the 25th ACM/IEEE conference on Design automation June 1988 This paper presents a new method for verifying functionality in the design of VLSI circuits. Our method fits naturally in a methodology based on a Hardware Description Language (HDL). Two programs describe the system under design: (1) its specification and (2) the extracted behaviour from its layout. Verifying the design comes down to proving that these programs are correct and equivalent with regard to the HDL semantics. We define a process named F	77%
8 4	An automated BIST approach for general sequential logic synthesis C. E. Stroud Proceedings of the 25th ACM/IEEE conference on Design automation June 1988 An automated Built-In Self-Test (BIST) technique for general sequential logic is described. This BIST approach has been incorporated in a behavioral model synthesis system providing automated implementation of BIST in Very Large Scale Integration (VLSI) devices as well as Programmable Logic used at all levels of testing from device testing through system diagnostics. The BIST approach is based on selective replacement of existing system memory elements with BIST flip-flop cells that are con	77%
9 [4]	Watermarking techniques for intellectual property protection A. B. Kahng , J. Lach , W. H. Mangione-Smith , S. Mantik , I. L. Markov , M. Potkonjak , P. Tucker , H. Wang , G. Wolfe Proceedings of the 35th annual conference on Design automation conference May 1998 Digital system designs are the product of valuable effort and know-how. Their embodiments, from software and HDL program down to device-level netlist and mask data, represent carefully guarded intellectual property (IP). Hence, design methodologies based on IP reuse require new mechanisms to protect the rights of IP producers and owners. This paper establishes principles of watermarking-based IP protection, where a watermark is a mechanism for identificatio	77%
	Partitioning algorithm to enhance VLSI testability Bassam Shaer , Sami A. Al-Arian , David Landis Proceedings of the 36th annual Southeast regional conference April 1998	77%
11	More wires and fewer LUTs: a design methodology for FPGAs Atsushi Takahara , Toshiaki Miyazaki , Takahiro Murooka , Masaru Katayama , Kazuhiro Hayashi , Akihiro Tsutsui , Takaki Ichimori , Kennosuke Fukami Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays March 1998 In designing FPGAs, it is important to achiev e a good balance bet ween the number of logic blocks, such has Look-Up Tables (LUTs), and wiring resources. It is difficult to find an optimal solution. In this paper, we present an FPGA design methodology to efficiently find well-balanced FPGA architectures. The method covers all aspects of FPGA development from the architecture-decision process to physical implementation. It has been used to develop a new FPGA that can implement circuits t	77%
12	Gate-level test generation for sequential circuits Kwang-Ting Cheng ACM Transactions on Design Automation of Electronic Systems (TODAES) October 1996 Volume 1 Issue 4 This paper discusses the gate-level automatic test pattern generation (ATPG) methods and techniques for sequential circuits. The basic concepts, examples, advantages, and limitations of representative methods are reviewed in detail. The relationship between gate-level sequential circuit ATPG and the partial scan design is also discussed.	77%
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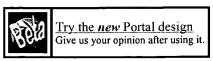
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Synthesis and optimization procedures for robustly delay-fault testable combinational logic circuits Srinivas Devadas, Kurt Keutzer Conference proceedings on 27th ACM/IEEE design automation conference January 1991 In this paper we apply recently developed necessary and sufficient conditions for robust path-delay-fault testability to develop synthesis procedures which produce two-level and multilevel circuits with high degrees of robust path delay fault testability. For circuits which can be flattened to two levels, we give a covering procedure which optimizes for robust path delay fault testability. These two-level circuits can then be algebraically factored to produ	77%
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ACM Transactions on Modeling and Computer Simulation (TOMACS) October 1991

Volume 1 Issue 4

We explore the suitability of the Chandy-Misra-Bryant (CMB) algorithm for the domain of digital logic simulation. Our evaluation is based on results for six realistic benchmark circuits, one of them being the R6000 microprocessor form MIPS. A quantitative evaluation of the concurrency exhibited by the CMB algorithm shows that an average of 42-196 element activations can be evaluated in parallel if arbitrarily many processors are available. One major factor limiting the parallel performance \dots

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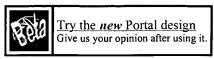
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SCAT—a new statistical timing verifier in a silicon compiler system

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M. Glesner , J. Schuck , R. B. Steck

Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986

The program SCAT is a new timing verifier within the ALGIC silicon compiler. It provides a precise assessment of the timing behaviour of the automatically generated LSI circuits by means of block-oriented statistical algorithms leading to a running time approximately linear to the number of circuit elements, which are emulated by delay time elements. Interconnect delays are handled by the same statistical model. Synchronous circuits are described by an appropriate coordinate transformation ...

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We explore the suitability of the Chandy-Misra-Bryant (CMB) algorithm for the domain of digital logic simulation. Our evaluation is based on results for six realistic benchmark circuits, one of them being the R6000 microprocessor form MIPS. A quantitative evaluation of the concurrency exhibited by the CMB algorithm shows that an average of 42-196 element activations can be evaluated in parallel if arbitrarily many processors are available. One major factor limiting the parallel performance ...

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1 On fault-simulation through embedded memories on large industrial designs

Yadavalli, S.; Kundu, S.;

VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001

Page(s): 117 -121

[Abstract] [PDF Full-Text (296 KB)] IEEE CNF

2 SymSim: symbolic fault simulation of data-flow data-path designs at the Register-Transfer

Yadavalli, S.; Reddy, S.M.;

Test Conference, 1999. Proceedings. International, 28-30 Sept. 1999

Page(s): 606 -615

[Abstract] [PDF Full-Text (836 KB)] IEEE CNF

3 Impact and cost of modeling memories for ATPG for partial scan designs

Yadavalli, S.; Sengupta, S.;

VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on , 4-7 Jan. 1998

Page(s): 274 -278

[Abstract] [PDF Full-Text (540 KB)] IEEE CNF

4 FX!32 a profile-directed binary translator

Chernoff, A.; Herdeg, M.; Hookway, R.; Reeve, C.; Rubin, N.; Tye, T.; Bharadwaj Yadavalli, S.; Yates, J.;

Micro, IEEE, Volume: 18 Issue: 2, March-April 1998

Page(s): 56 -64

[Abstract] [PDF Full-Text (172 KB)] IEEE JNL

5 MUSTC-Testing: Multi-Stage-Combinational Test scheduling at the Register-Transfer Level

Yadavalli, S.; Pomeranz, I.; Reddy, S.M.;

VLSI Design, 1995., Proceedings of the 8th International Conference on , 4-7 Jan. 1995

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1 Circuit and platform design challenges in technologies beyond 90nm

Grundmann, B.; Galivanche, R.; Kundu, S.;

Design, Automation and Test in Europe Conference and Exhibition, 2003, March 3-7, 203

Page(s): 44 -47

[Abstract] [PDF Full-Text (679 KB)] IEEE CNF

2 On modeling cross-talk faults

Zachariah, S.T.; Yi-Shing Chang; Kundu, S.; Tirumurti, C.;

Design, Automation and Test in Europe Conference and Exhibition, 2003, March 3-7, 203

Page(s): 490 -495

[Abstract] [PDF Full-Text (270 KB)] IEEE CNF

3 On the characterization of hard-to-detect bridging faults

Pomeranz, I.; Reddy, S.M.; Kundu, S.;

Design, Automation and Test in Europe Conference and Exhibition, 2003, March 3-7, 203

Page(s): 1012 -1017

[Abstract] [PDF Full-Text (249 KB)] IEEE CNF

4 On output response compression in the presence of unknown output values

Pomeranz, I.; Kundu, S.; Reddy, S.M.;

Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002

Page(s): 255 -258

[Abstract] [PDF Full-Text (538 KB)] IEEE CNF

5 Finite-state modeling in software design: some fundamental techniques

Kundu, S.;

Software Engineering Conference, 2002. Ninth Asia-Pacific, 4-6 Dec. 2002

Page(s): 317 -324

[Abstract] [PDF Full-Text (248 KB)] IEEE CNF

6 Role of buffer layers in CIS-based solar cells

Olsen, L.C.; Eschbach, P.; Kundu, S.;

Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE , May 19-24, 2002 Page(s): 652 -655

[Abstract] [PDF Full-Text (329 KB)] IEEE CNF

7 Chemical bath dep sited (CBD) ZnS buffer layer for CIGSS solar cells

Kundu, S.; Olsen, L.C.;

Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE , May 19-24, 2002 Page(s): 648 -651

[Abstract] [PDF Full-Text (300 KB)] IEEE CNF

8 Call bl cking in a mobile radio system with directed retry and priority handoff

Kundu, S.; Chakrabarti, S.;

Personal Wireless Communications, 2002 IEEE International Conference on , Dec. 15-17, 2002

Page(s): 163 -167

[Abstract] [PDF Full-Text (342 KB)] IEEE CNF

9 Resource allocation in DS-CDMA with imperfect power control and correlated interference

Kundu, S.; Chakrabarti, S.;

Personal Wireless Communications, 2002 IEEE International Conference on , Dec. 15-17, 2002

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[Abstract] [PDF Full-Text (342 KB)] IEEE CNF

10 Genetic algorithm application to vibration control of tall flexible structures

Kundu, S.; Seto, K.; Sugino, S.;

Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Workshop on , 29-

31 Jan. 2002

Page(s): 333 -337

[Abstract] [PDF Full-Text (532 KB)] IEEE CNF

${f 11}$ On fault-simulation through embedded memories on large industrial designs

Yadavalli, S.; Kundu, S.;

VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001

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[Abstract] [PDF Full-Text (296 KB)] IEEE CNF

12 Fast statistical timing analysis by probabilistic event propagation

Jing-Jia Liou; Kwang-Ting Cheng; Kundu, S.; Krstic, A.;

Design Automation Conference, 2001. Proceedings , 18-22 June 2001

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[Abstract] [PDF Full-Text (616 KB)] IEEE CNF

13 The canonical functional design based on the domination-relationship among data

Kundu, S.;

Software Engineering Conference, 2001. APSEC 2001. Eighth Asia-Pacific , 4-7 Dec 2001

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[Abstract] [PDF Full-Text (733 KB)] IEEE CNF

14 Minimum duration outage analysis of cellular CDMA for integrated services with correlated signal and interference

Kundu, S.; Chakrabarti, S.;

Personal Wireless Communications, 2000 IEEE International Conference on , 17-20 Dec. 2000

Page(s): 254 -258

[Abstract] [PDF Full-Text (232 KB)] IEEE CNF

15 Outage analysis of cellular CDMA for integrated voice and data services with correlated signal and interference

Kundu, S.; Chakrabarti, S.;

Personal Wireless Communications, 2000 IEEE International Conference on , 17-20 Dec. 2000

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[Abstract] [PDF Full-Text (276 KB)] IEEE CNF

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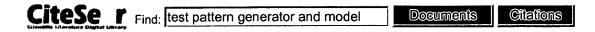
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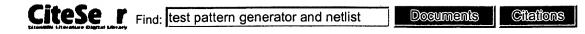
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Optimal Hardware Pattern Generation for Functional BIST - Silvia Cataldo Silvia (2000) (Correct) (1 citation) sequential module to be used as hardware test pattern generator. Up to now, only linear feedback shift are fully accessible, e.g. via full scan The netlist of the UUT is available Single stuck-at ATPG Post Processor Optimization parameters UUT netlist Optimal triplets set Instrumented Test Set ftp.ra.informatik.uni-stuttgart.de/pub/pdf/date00.pdf

DELTEST: Deterministic Test Generation for Gate Delay Faults - Udo Mahlstedt Institut (1993) (Correct) (2 citations) fanout branches. algorithms. The stuck-at test pattern generator A complete test set generated for a delay tools operate on a common data base. The internal netlists are generated by a tool called EDNET. EDNET generated by a tool called EDNET. EDNET converts netlist descriptions from EDIF 2.0.0 to the internal www.tet.uni-hannover.de/papers/1993/93umah 1.ps

A new functional fault model for FPGA.. - Rebaudengo, Reorda.. (Correct) presented the adoption of a classical Test Pattern Generator [6] considering a modified gate level are proposed in order to simplify the circuit netlist and eliminate redundant faults corresponding to apply the proposed fault model, the obtained VHDL netlist has been modified substituting each LUT with its www.cad.polito.it/pap/db/dft2002a.pdf

Internet-based Collaborative Test Generation with MOSCITO - Schneider Ivask Miklos (Correct) of a tool (e.g. fault simulator, a test pattern generator, a netlist translator, to a (e.g. fault simulator, a test pattern generator, a netlist translator, to a potential user as a (e.g. fault simulators, test pattern generators, netlist translators) with MOSCITO a sophisticated agent www.sigda.org/Archives/ProceedingArchives/Date/Date2002/papers/2002/date02/htmfiles/sun_sqi/../../pdffiles/02e_2.pdf

VHDL Fault Simulation for Defect-Oriented Test and .. - Celeiro, Dias.. (1996) (Correct) and iceTgen (gate-level realistic test pattern generator and fault simulator)The tools Such heuristic, based on the gate-level circuit netlist, aims at deriving a PSR fault set which mimics, 1984. 21] F. Brglez, H. Fujiwara, A Neutral **Netlist** of 10 Combinational Benchmark Circuits and a herkules.informatik.tu-chemnitz.de/proceedings/eurodac-96/papers/1996/eurdac96/htmfiles/sun sgi/../../pdffiles/v04 2.pdf

Operating System Support for Cooperation in Distributed OODBs - Dinesh Kulkarni Arindam (1992) (Correct) of" a hinge and a gripper and so on. Test Pattern Generator Stimuli Device Model Parameters Netlist object has references to four passive objects: a netlist indicating circuit topology the device model Pattern Generator Stimuli Device Model Parameters Netlist Circuit Simulator Circuit Performance Device www.cse.nd.edu/pub/Reports/1992/tr-92-4.ps.gz

A Test Pattern Generation Algorithm Exploiting Behavioral.. - Silvia Chiusano Fulvio (Correct) of gates is prohibitively expensive. Test pattern generators, alone, cannot cope with the complexity about circuit behavior when the gate level netlist, only, is available. Gatelevel algorithms are test patterns are applicable to gate-level netlists. Information gathered at the RT-level is www.cad.polito.it/pap/db/ats98.ps.gz

A Genetic Algorithm for Automatic Generation of Test Logic.. - Fulvio Corno Paolo (1996) (Correct) sequences can be generated by Automatic Test Pattern Generators, but hardware structures able to of the Cellular Automaton starting from the netlist of the addressed FSM. Section 4 reports some model is adopted. Our algorithm reads the FSM netlist and the fault list, and chooses a rule for each www.cad.polito.it/pap/db/ictai96.ps.gz

<u>Decision Diagram Synthesis from VHDL - Jervan (1998) (Correct)</u> synthesis. The hierarchical Automatic Test Pattern G nerator (ATPG) operates with the Structurally (VHDL) Logic-level synthesis (SYNOPSYS) Gate-level netlist (EDIF) DD-based test generation system Figure 1 SSBDDs will be created from the gate-level netlist. Current system uses for logic level synthesis

www.pld.ttu.ee/magister/thesis.pdf

Functional Decompositions Using an Automatic Test Pattern.. - Tsutomu Sasao And (1999) (Correct) Decompositions Using an Automatic Test Pattern Generator and a Logic Simulator Tsutomu Sasao and and a logic simulator. Since the method uses netlists rather than binary decision diagrams to it can decompose larger networks. By using netlists, it efficiently finds decompositions of form www.lsi-cad.com/sasao/Papers/files/IWLS1999 kajihara.pdf

Cellular Automata for Deterministic Sequential Test.. - Silvia Chiusano Fulvio (1997) (Correct) and to propose a har dware deterministic test pattern generator for sequential embedded circuits, when the Cellular Automaton starting from the netlist of the circuit to be tested. Se ction 4 reports shown in Fig. 3: our algorithm reads the circuit netlist and the fault list, and it chooses with a GA a www.cad.polito.it/pap/db/vts97.ps.gz

RID-GRASP: Redundancy Identification and Removal Using GRASP - Joonyoung Kim Joo (Correct) removal system, RIDGRASP, is based on this test pattern generator that we call TG-GRASP. The use of GRASP is shown in Figure 3. RID-GRASP reads in a netlist C and a fault list F, and writes back an F, and writes back an equivalent redundancy-free netlist. Basically, its operation consists of targeting algos.inesc.pt/pub/users/jpms/papers/iwls97/rid-grasp.ps.gz

Advanced ATPG for Delay-Faults in CPLDs - Kerkhoff, Sachdev, Speek (Correct) developed and integrated in a delay-fault test-pattern generator. The approach is based on extensive speed behaviour. Hence, only part of the complete netlist is used for determining the critical timing circuit simulator and the layout-extracted netlists of the primitives and non-primitives including www.stw.nl/prorisc/cssp97/proc/psz/kerkhoff2.ps.gz

A Complete Test Strategy Based on Interacting and Hierarchical.. - Fummi, Sciuto (Correct) level. 1 Introduction Any sequential test pattern generator [7, 8, 9] is constrained to explore analysis is performed at gate level on the flat netlist, without taking into account information on the ipeca4.elet.polimi.it/pub/paper/fs97c.ps.gz

A Comprehensive Partial Scan Chain Assignment and Test Generation - Clay Gloster (1995) (Correct) fault set F hard .A combinational test pattern generator [15, 16] finds combinational tests for Weights Aaaaa Aaaaa Faultlist F Om Aaa Aaa Om Netlist Aaaaaa Aaaaaa Functional And Random www.cbl.ncsu.edu/publications/1995-TR@CBL-02-Gloster/1995-TR@CBL-02-Gloster.ps.gz

An Analysis of Shorts in CMOS Standard Cell Circuits - Alvin Jee (1994) (Correct) level and few fault simulators and test pattern generators can deal with faults at the transistor are extracted (location in the layout and in the netlist)the characteristics and behaviors of the the interconnect faults as well as a gate level netlist for the circuit. To extract the gate level ftp.cse.ucsc.edu/pub/tr/ucsc-crl-94-41.ps.Z

A Testing Methodology for VHDL Based High-Level Designs - Buonanno, Ferrandi, Fummi, ... (Correct) usually considered by most commercial test pattern generators and design for testability tools. This by means of a structured set of behaviors and netlists. Behaviors are represented by architectures i.e. modules with well specified I/O interfaces. Netlists are represented by architectures specifying the ipeca4.elet.polimi.it/pub/paper/bff97b.ps.gz

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An Timing Driven Pseudo Exhaustive Testing for VLSI Circuits - Chang And Rau (Correct) exhaustive testing, two components -a test pattern generator (TPG) and an output response analyzer The basic structure of a bsc contains a mux and a flip-flop in Fig. 2. During the normal mode, the signal, can reduce the test time, it may increase circuit delay. In this paper, our objective is to reduce the www.cs.ccu.edu.tw/~scchang/papers/pseudo_test_jour.pdf

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Minimizing Power Dissipation in Combinational Circuits.. - Dabholkar, Chakravarty (1994) (Correct) environment[7] or when a special built-in test pattern generator is designed for the circuit under were proposed. They are: Test set ordering and Flip-Flop ordering. Here we address this problem for Power dissipation is a function of the circuit delay. Three delay models have been studied in the ftp.cs.buffalo.edu/pub/tech-reports/94-10.ps.Z

Cost/Quality Trade-off in High-Level Synthesis for.. - Bukovjan, Marzouki, Maroufi (1998) (Correct) must generate the circuit integrating a Test Pattern Generator (TPG) and Test Result Checker (TRC)A ADEPT [16] performing intelligent partial scan flip-flop selection based on RTL information and AMBIANT the partial scan technique to reduce the area and delay overhead. The Gu et al. system use as well test asim.lip6.fr/pub/reports/1998/ar.buk.ddecs98.ps.gz

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